

**Notice of Allowability**

Application No.

09/880,621

Examiner

Daniel Pan

Applicant(s)

DRYSDALE ET AL.

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the amendment filed on 09/15/04.
2. ☒ The allowed claim(s) is/are 4-9, 13-15, 23, 25-28, 30-36, 41-44, 58, 60-65, 67 and 68.
3. ☒ The drawings filed on 07 January 2002 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some\* c) ☐ None of the:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.  
(a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached  
1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.  
(b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.  
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)  
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08),  
Paper No./Mail Date \_\_\_\_\_  
4. ☐ Examiner's Comment Regarding Requirement for Deposit  
of Biological Material  
5. ☐ Notice of Informal Patent Application (PTO-152)  
6. ☐ Interview Summary (PTO-413),  
Paper No./Mail Date \_\_\_\_\_  
7. ☐ Examiner's Amendment/Comment  
8. ☒ Examiner's Statement of Reasons for Allowance  
9. ☐ Other \_\_\_\_\_

DANIEL H. PAN  
PRIMARY EXAMINER  
GROUP 103

## Reasons for Allowance

Claims 1-3, 10-12,16-22, 24,29,37-40,45-57,59,66 have been canceled.

None of the prior art of record teaches :

1. the combined features of the first register communicating from a first core (or thread) to second core, wherein the first register was decoded by the first core to have a first register name and was decoded by the second core to have a second register name, and the second register communicating from the second core to the first core, wherein the second register was decoded by the first core to have the second register name and decoded by the second core to have the first register name (claims 4,13,);
2. the combined features of cores (threads) , each associated with a read only register to receive information relating to another core and a read –write register to output information used by another core, the logic operation to the contents of read-write register of each core and the storage of the result in the read-only register of each core (claims 23,28,33,41);
3. the combined features of the first register for communicating **only** from the first core to second core, wherein the first register included bits used to synchronize operation of the first core and second code, and the second register to communicate **only** from the second core to the first core, wherein the second register included a plural bits used to synchronize operation of the first core and second core (Claims 58, 65 );

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4. the combined features of the first register communicating information from the first entity to second entity of a microprocessor, the second register for communicating the information from the second entity to the first entity, the means for cross decoding the first register and second register, the means causing the first entity to set the predetermined bit in the first register, and the means for causing the first processing entity to wait until the corresponding bit in the second register is set before proceeding (claim 62).

#### References of Record

5. Torii (5,913,059) was used for showings teaching a plurality of processing entities, or threads (see fig.9 [21a][21b], see the parallel processing of the threads in cool.8, lines 34-42) having associated with a first register [27a] and second register [24a], and the logic operation (see output lines from the 24a in the entity 21a and from 24 b in entity 21b). However, it did not teach the first register was a read-only register and the second register was a read-write register as claimed (e.g. see claims 23,28,33,41).

6. Levy et al. (6,092,175) was used to show first processing entity (first thread) and a second processing entity (second thread), the first register (see any shared register in the register pool), the second register (see any other shared register in the register pool) the communication (fig.5 D) between the first processing entity and second processing entity, and the cross decoded of the first entity and second entity (col.10, lines 42-52, see also col.10, lines 5-17 for the renaming registers shared across the threads, see

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also the mapping in the renaming table in col.9, lines 22-32 for the background teaching of mapping). However, it failed to show a single microprocessor and the means for causing the first processing entity to wait until a corresponding bit in the second processing register was set before proceeding (claim 62).

7. Delaruelle et al. (5,095,523) was used to supplement the teaching of bit wise operation. However, it did not teach the first register was a read-only register and the second register was a read-write in addition to the plurality of processing cores, each having the read-only and read-write register.

8. Schimmel (6,496,909) was used to show the first core (see the thread for requesting the access in col.9, lines 29-35), the second core (see the additional competing threads), a register (shared by the threads) which included a bit [lock bit] used to synchronize the operation of the first and second cores (col.9, lines 29-46, fig.5 entries of memory table storing the lock bit in col.10, lines 25-41). However, it failed to show the first register communicated information only from the first core to second core, and the second register communicated information only from the second core to the first core (e.g. see claim 58).

9. Manabe (5,590,326) was used for showing the teaching of a first register [520 lock set up unit] and a second register [520 lock set up unit] and a means for cross decoding the first register and second register between the first processing entity [50 left] and second processing entity [50 right]. However, it failed to show the first register

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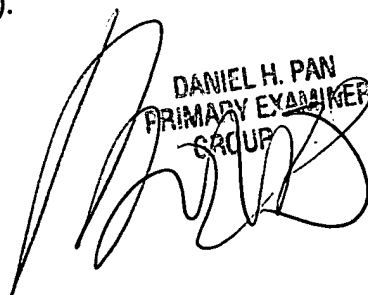
communicated information only from the first core to second core, and ht second register communicated information only from the second core to the first core (e.g. see claims 13, 65).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**21 Century Strategic Plan**

  
DANIEL H. PAN  
PRIMARY EXAMINER  
GROUP